IN THE SPECIFICATION:

(A) On page 1, before the "BACKGROUND OF THE INVENTION" section, please add the following new section:

--RELATED APPLICATION DATA

This application is a divisional of U.S. Patent Appln. No. 09/404,920, filed on September 24, 1999, in the names of Frederic Reblewski, Olivier LePape, and Jean Barbier. This present application is entirely incorporated herein by reference.--.

(B) Please amend the paragraph at page 10, lines 8-13 as follows:

Preferably, FPGA **100** also includes memory **112**, context bus **106**, scan register **108**, and trigger circuitry **110**. Memory **112** facilitates usage of FPGA **100** to emulate circuit designs with memory elements. Context bus **106**, scan register **108** and trigger circuitry **110** provide on-chip integrated debugging facility for FPGA **100**. These elements are described in U.S. ~~patent application serial number~~ Patent Appln. No. 08/542,838, entitled "A Field Programmable Gate Array with Integrated Debugging Facilities," ~~,~~ which is hereby fully incorporated by reference.

(C) Please amend the paragraph at page 15, lines 14-19 as follows:

In an alternate embodiment of the present invention, signals are routed directly from I/O pins ~~510~~ 518 of FPGA **501** to/from I/O pins **533** of FPGA **503** without being routed through RC **502**. I/O circuitry **515** and **536** are both clocked by one of either signal routing clock **509** or signal routing clock **510**. Thus, even though a routing chip is not used in this alternate embodiment, the signal routing between FPGAs is still clocked by a signal independent of the user clock signal(s).

(D) Please amend the paragraph at page 22, line 17 through page 23, line 6 as follows:

Chips **1102** and **1104** can simultaneously transfer signals to each other via connection **1108**. Chips **1102** and **1104** each include I/O circuitry, including a driver and ~~a~~ detection logic as illustrated. An output signal **1121** to be output by chip **1102** is driven onto connection **1108** via driver ~~**1122**~~ **1123**. Concurrently, an output signal **1132** to be output by chip **1104** is driven onto connection **1108** via driver **1133**. After the signals are driven onto connection **1108**, detection logics **1125** and **1135** each sample the voltage level of connection **1108**. Based on the sampled voltage level of connection **1108**, as well as possibly the output signal **1132**, detection logic **1135** provides an input signal **1131** to the internal circuitry of chip **1104**, which is representative of output signal **1121** driven by chip **1102**. Similarly, based on the sampled voltage level of connection **1108**, as well as possibly the output signal **1121**, detection logic **1125** provides an input signal **1122** to the internal circuitry of chip **1102**, which is representative of output signal **1132** driven by chip **1104**.